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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/813,035	03/21/2001	Masanari Asano	024354-00001	2760

7590 03/14/2006

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EXAMINER	
NGUYEN, KIMBINH T	
ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/813,035	ASANO, MASANARI	
	Examiner	Art Unit	
	Kimbinh T. Nguyen	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/06/06 has been entered.

1. This action is responsive to amendment filed 01/06/06.

2. Claims 1-21 are pending in the application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Glennon et al. (5,805,173).

Claims 1 and 16, Glennon et al. discloses an image processor (CPU 104), comprising: a storage circuit storing therein image data (display memory 110; col. 4, lines 22-28); a memory control circuit comprising an address generation circuit generating an address in said storage circuit to and from which the image data is written in and read out (col. 14, lines 11-12), said memory control circuit comprising an area

adjustment circuit which sets up an additional area adjacent to an area in which the image data are actually stored in a memory space of said storage circuit and storing therein additional data other than the image data, which adjust the address generated by said address generation circuit, and which reads out the image data from said storage circuit, including the additional data in the additional area, in response to the address and a read control signal supplied to said storage circuit, wherein the additional data are written in with an address of the additional area (col. 14, lines 13-50); a data input/output circuit controlling input/output of the image data (media stream controller 414); an access control circuit controlling access of writing in and reading out the image data to and from said storage circuit (video input controller); a refresh circuit controlling refreshing of said storage circuit (a memory refresh module 508; fig. 5; col. 12, lines 66-67).

Claim 2, Glennon et al. discloses wherein said area adjustment circuit sets up the additional area immediately preceding or following the area in which the image data is stored (col. 14, lines 21-67).

Claim 3, Glennon teaches information on a position of the additional area is supplied as setting information included in header information (an additional 8 bits header information; col. 14, lines 21-28).

Claim 4, Glennon et al. teaches the area adjustment circuit set a size of the additional area using information ((an additional 8 bits of control information), which is obtained in synchronization with a supplied vertical synchronization signal (on a separate 8 bit line; col. 13, lines 46-67), as a parameter and reads out the data stored in

the additional area in response to a data transfer request (col. 13, line 42 through col. 14, line 50).

Claims 5-7, Glennon et al discloses wherein said area adjustment circuit obtains information on a base point in the memory space, a row direction width (a line), and a column direction width (vertical lines) and outputs the obtained information to said address generation circuit as a parameter (col. 14, lines 13-67).

Claims 8-10,Glennon et al discloses wherein said area adjustment circuit supplies the additional data, which is read out from the additional area (an additional 8 bits), to a predetermined position in a video signal (col. 14, lines 22-50).

Claim 11, Glennon et al discloses wherein said access control circuit supplies the additional data other than the image data to said memory circuit (col. 4, lines 53-67).

Claims 12 and 17, Glennon et al discloses an image processing method comprising the steps of: setting up, in a storage circuit in which image data is stored 9byte stream decoder 203; fig. 4), a range of an image area in which the image data is written and a range of an additional area which is adjacent to the image area and in which data other than the image data is written (an additional 8 bits of control information), with information supplied to a memory space of said storage circuit as a parameter (col. 14, lines 13-24); writing the additional data other than the image data from external into the additional area in said storage circuit according to a first write control signal (col. 14, lines 21-40); writing the image data at an address location of the image area in said storage circuit according to a second write control signal (col. 14, lines 35-40); and reading out the additional data stored in the additional area and the

image data stored in the image area in said storage circuit in response to a first read control signal, wherein the additional data are written in with an address of the additional area (col. 14, lines 13-50).

Claim 13,Glennon et al discloses wherein said step of reading out the additional data comprises the steps of: reading out the additional data from the additional area in said storage circuit in response to the first read control signal (input controller 418); and reading out the image data from the image area in said storage circuit in response to a second read control signal (media stream controller 414; col. 14, lines 21-40).

Claim 14, Glennon et al. teaches the first write control signal (the control logic 209) and the read control signal (video input controller 418) are a transfer enable signal enabling an execution of processing (col. 14, line 51 through col. 16, line 38; table 6).

Claim 15, Glennon et al discloses wherein said step of reading out the additional data inserts the additional data read out from the additional area into a predetermined position of a video signal (col. 14, line 41 through col. 9).

Claims 18-20, Glennon et al discloses wherein said additional area has an adjustable width (col. 19, lines 1-29).

Claim 21, the rationale provided in the rejection of claims above is incorporated herein. In addition, Glennon et al. teaches the additional data are teletex data (col. 3, lines 53-55; col. 24, lines 3-6).

Response to Arguments

5. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimbinh T. Nguyen whose telephone number is (571) 272-7644. The examiner can normally be reached on Monday to Thursday from 7:00 AM to 4:30 PM. The examiner can also be reached on alternate Friday from 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached at (571) 272-7664. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 9, 2006

Kimbinh Nguyen

KIMBINH T. NGUYEN
PRIMARY EXAMINER